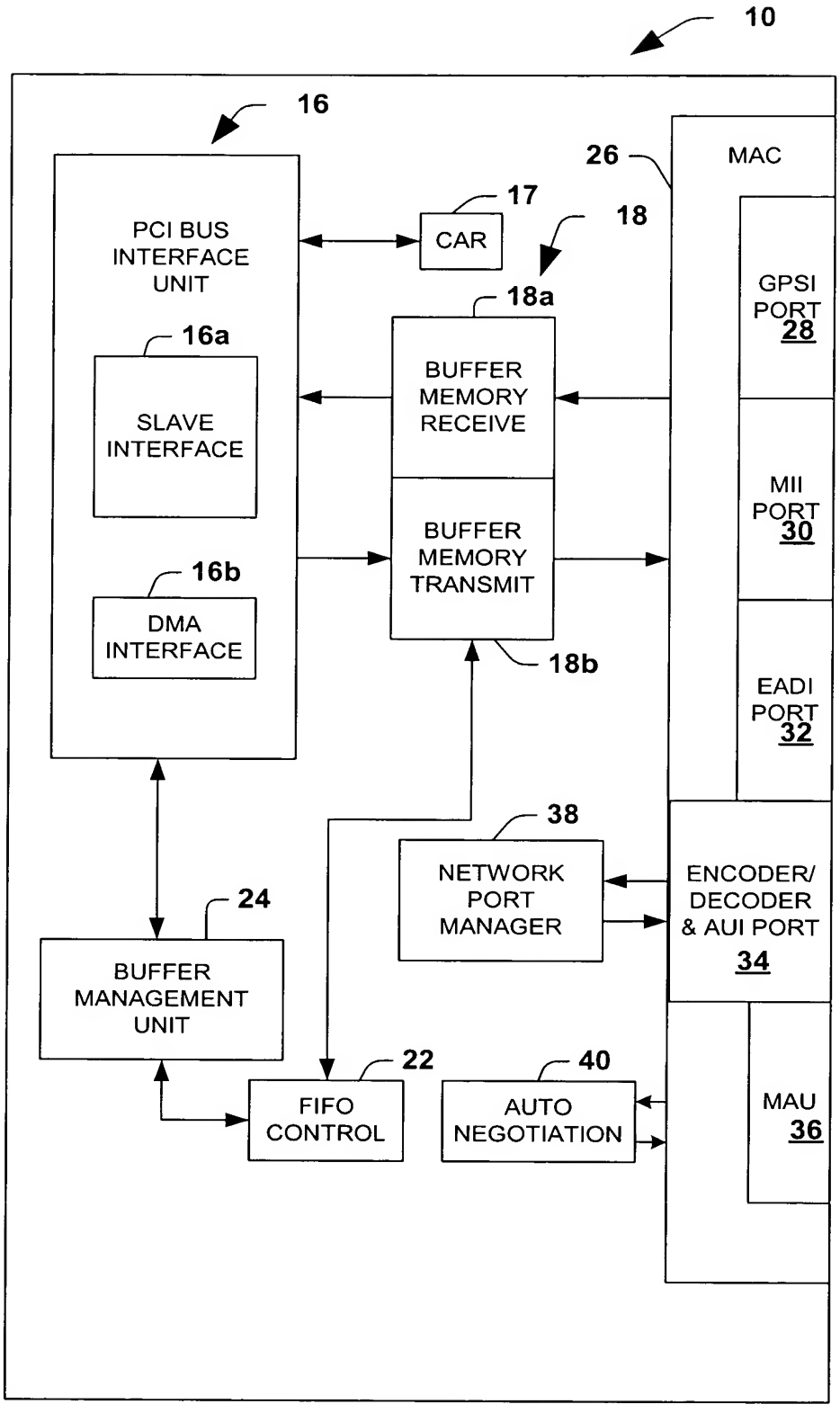

Fig. 1
(PRIOR ART)

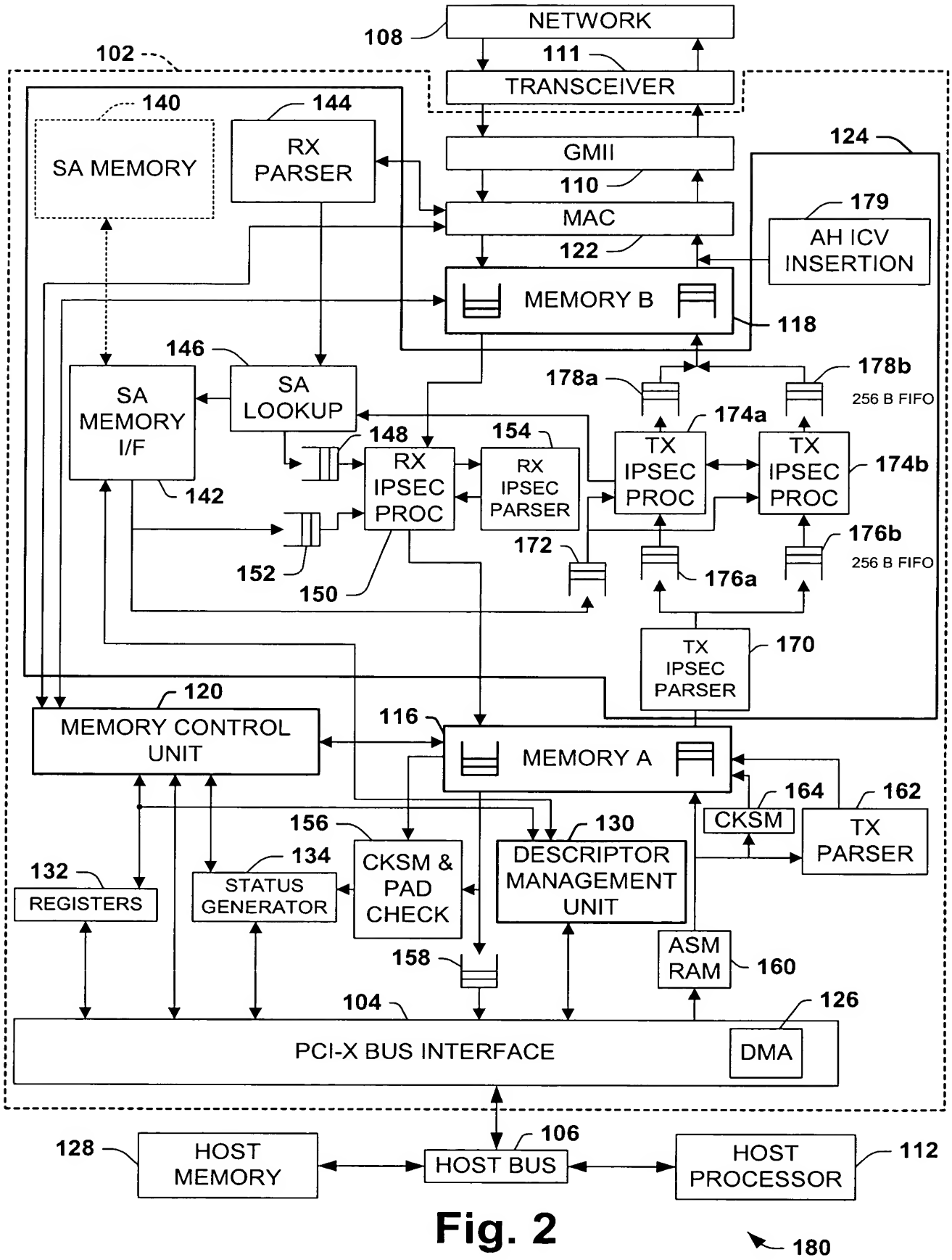
NETWORK
108
111
TRANSCEIVER
102
140
SA MEMORY
144
RX PARSER
GMII
110
MAC
122
124
179
AH ICV INSERTION
MEMORY B
118
146
SA LOOKUP
SA MEMORY I/F
142
178a
178b
256 B FIFO
174a
148
154
RX IPSEC PROC
RX IPSEC PARSER
TX IPSEC PROC
174b
152
150
172
176b
256 B FIFO
176a
TX IPSEC PARSER
170
120
MEMORY CONTROL UNIT
116
MEMORY A
164
CKSM
162
TX PARSER
156
130
132
134
REGISTERS
STATUS GENERATOR
CKSM & PAD CHECK
DESCRIPTOR MANAGEMENT UNIT
158
ASM RAM
160
104
126
PCI-X BUS INTERFACE
DMA
106
128
HOST MEMORY
HOST BUS
HOST PROCESSOR
112
180

Fig. 2

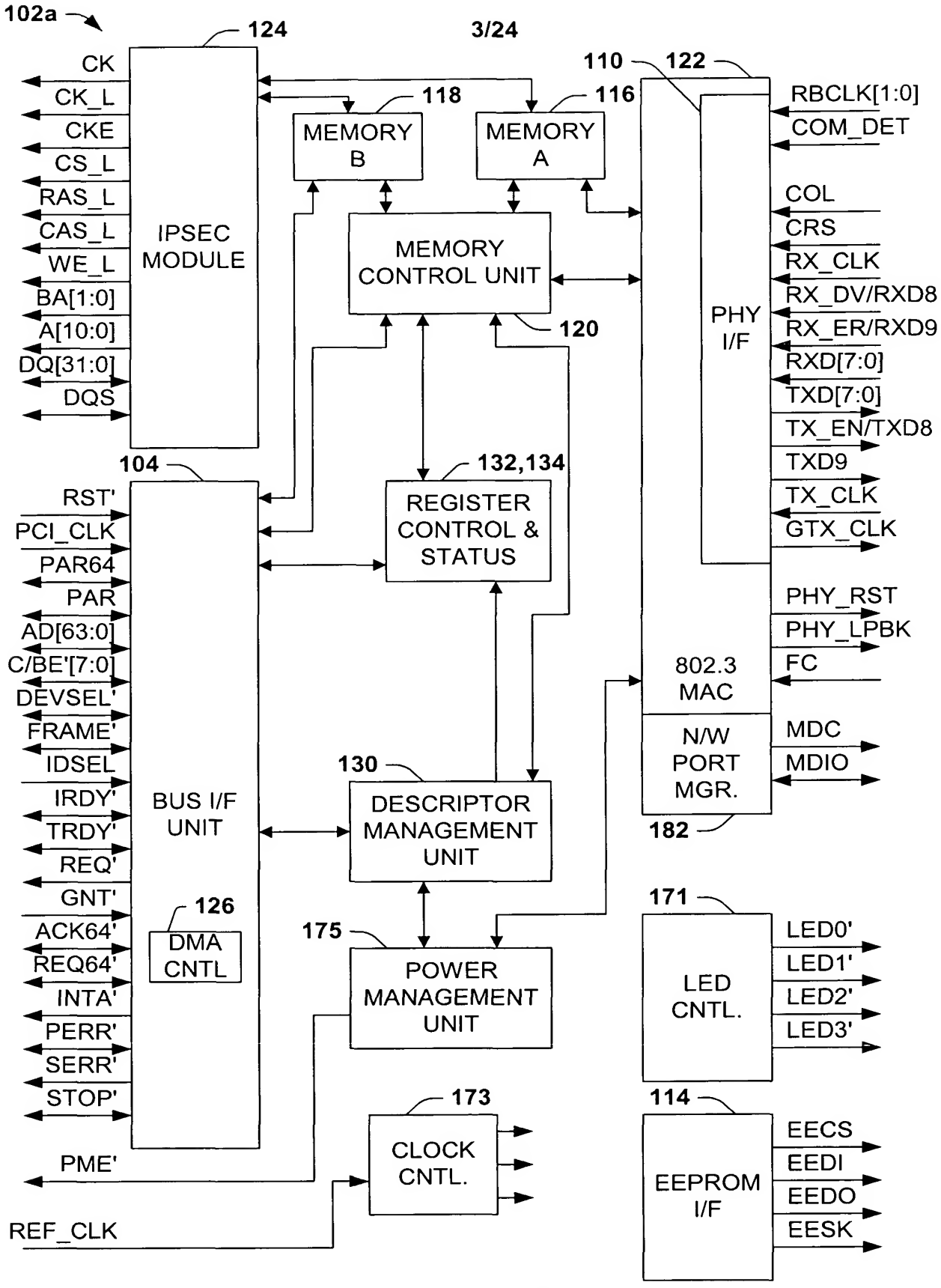
102a
124
CK
CK_L
CKE
CS_L
RAS_L
CAS_L
WE_L
BA[1:0]
A[10:0]
DQ[31:0]
DQS
IPSEC MODULE
118
MEMORY B
116
MEMORY A
MEMORY CONTROL UNIT
120
110
122
PHY I/F
RBCLK[1:0]
COM_DET
COL
CRS
RX_CLK
RX_DV/RXD8
RX_ER/RXD9
RXD[7:0]
TXD[7:0]
TX_EN/TXD8
TXD9
TX_CLK
GTX_CLK
104
RST'
PCI_CLK
PAR64
PAR
AD[63:0]
C/BE'[7:0]
DEVSEL'
FRAME'
IDSEL
IRDY'
TRDY'
REQ'
GNT'
ACK64'
REQ64'
INTA'
PERR'
SERR'
STOP'
BUS I/F UNIT
132,134
REGISTER CONTROL & STATUS
PHY_RST
PHY_LPBK
FC
802.3 MAC
N/W PORT MGR.
MDC
MDIO
182
130
DESCRIPTOR MANAGEMENT UNIT
126
DMA CNTL
175
POWER MANAGEMENT UNIT
171
LED CNTL.
LED0'
LED1'
LED2'
LED3'
173
CLOCK CNTL.
PME'
REF_CLK
114
EEPROM I/F
EECS
EEDI
EEDO
EESK

Fig. 3

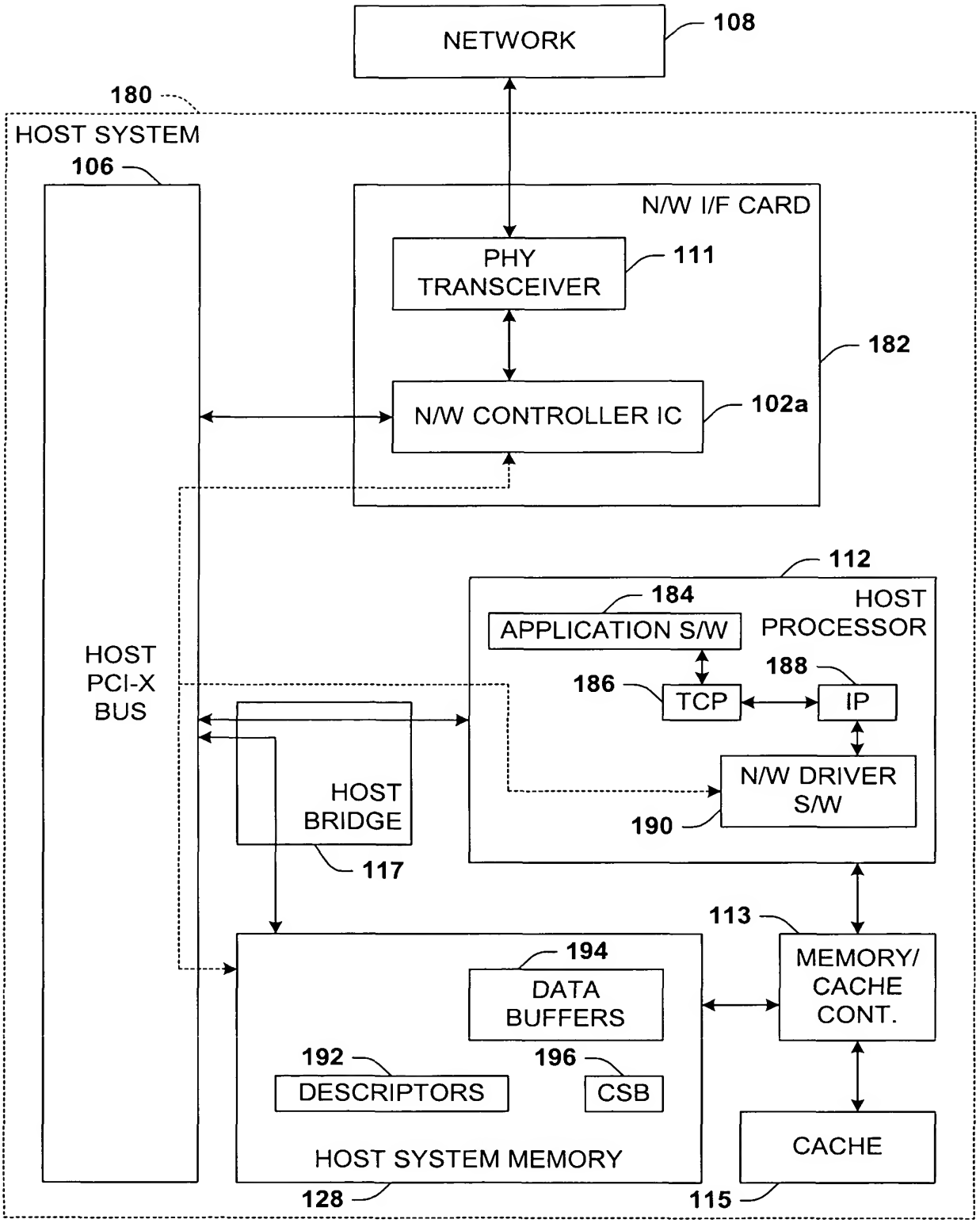
NETWORK
108
180
HOST SYSTEM
106
N/W I/F CARD
PHY
TRANSCEIVER
111
182
N/W CONTROLLER IC
102a
112
184
APPLICATION S/W
HOST
PROCESSOR
188
186
TCP
IP
HOST
PCI-X
BUS
N/W DRIVER
S/W
190
HOST
BRIDGE
117
113
194
DATA
BUFFERS
MEMORY/
CACHE
CONT.
192
196
DESCRIPTORS
CSB
HOST SYSTEM MEMORY
CACHE
128
115

Fig. 4

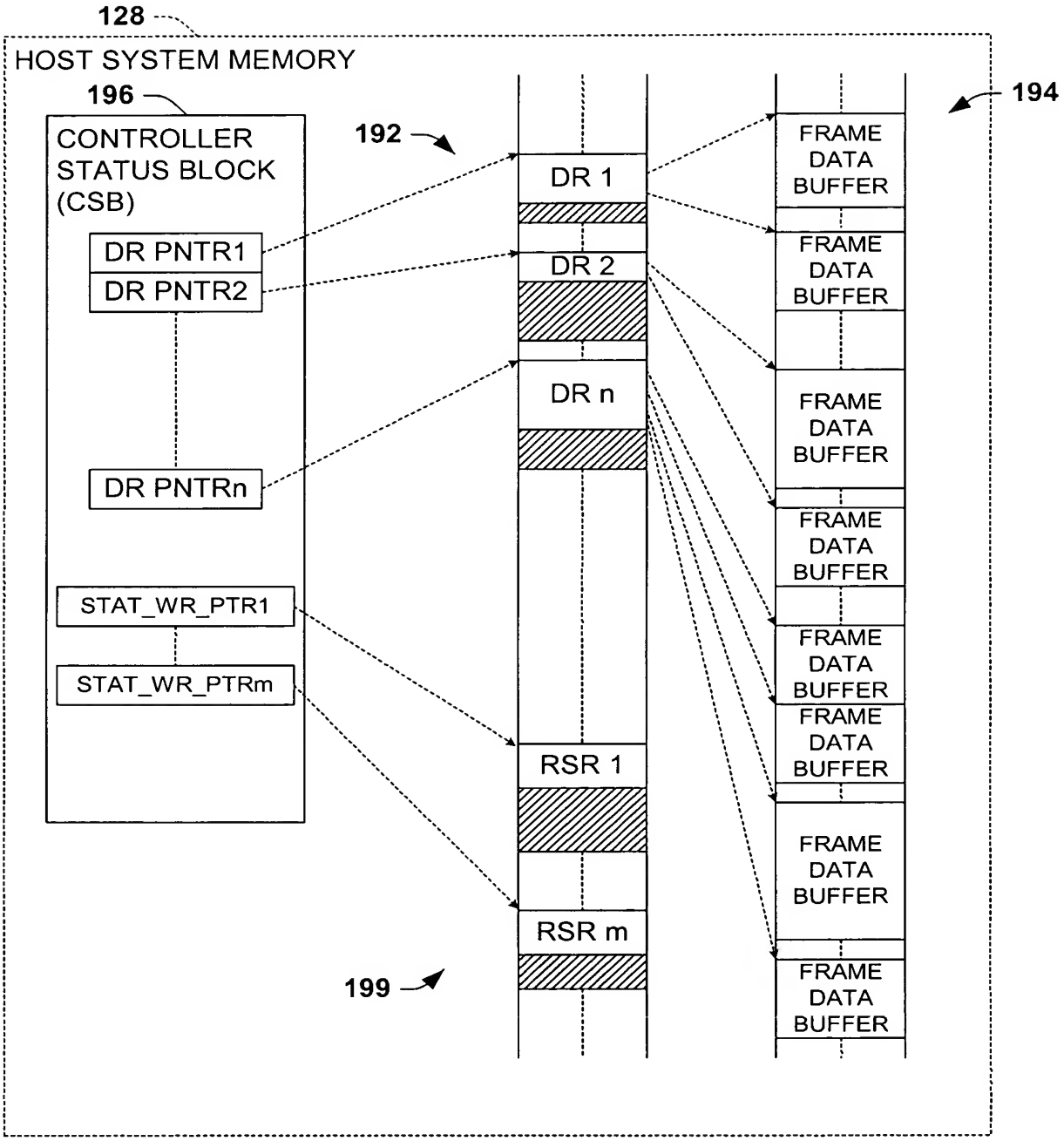
128
HOST SYSTEM MEMORY
196
CONTROLLER STATUS BLOCK (CSB)
DR PNTR1
DR PNTR2
DR PNTRn
STAT_WR_PTR1
STAT_WR_PTRm
192
DR 1
DR 2
DR n
RSR 1
RSR m
199
194
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER

Fig. 5A

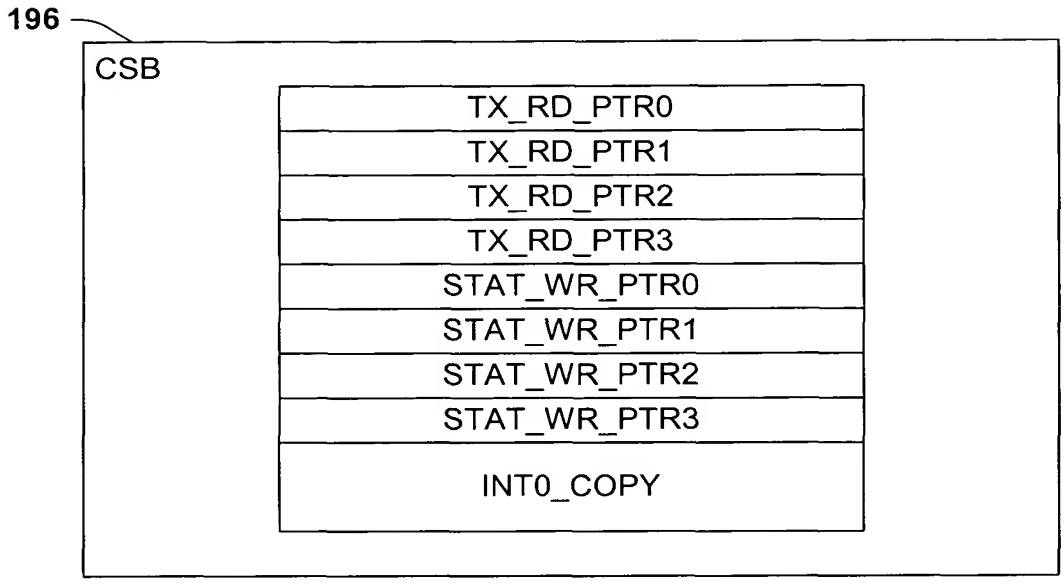
196
CSB
TX_RD_PTR0
TX_RD_PTR1
TX_RD_PTR2
TX_RD_PTR3
STAT_WR_PTR0
STAT_WR_PTR1
STAT_WR_PTR2
STAT_WR_PTR3
INT0_COPY

Fig. 5B

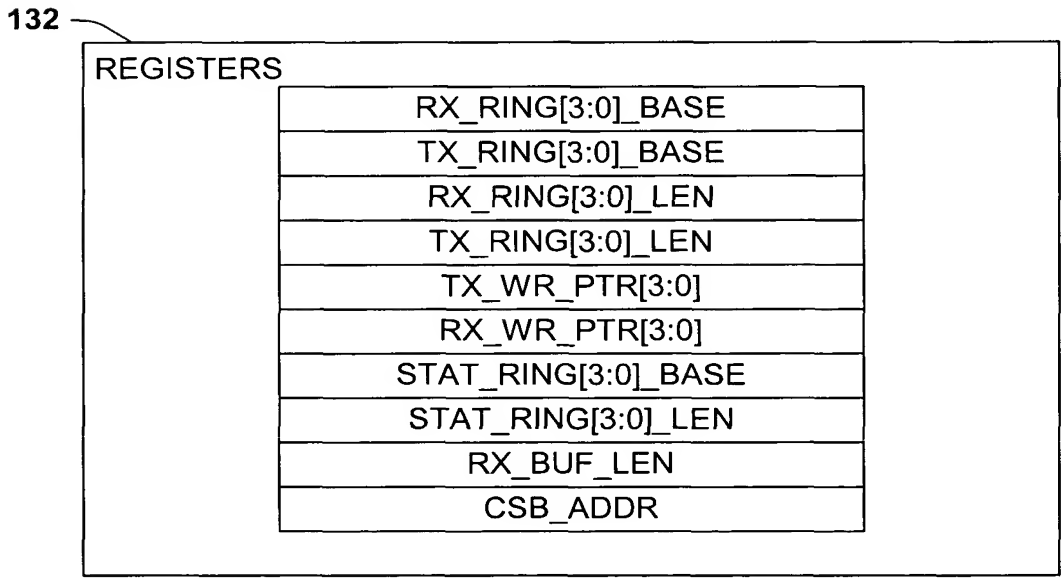
132
REGISTERS
RX_RING[3:0]_BASE
TX_RING[3:0]_BASE
RX_RING[3:0]_LEN
TX_RING[3:0]_LEN
TX_WR_PTR[3:0]
RX_WR_PTR[3:0]
STAT_RING[3:0]_BASE
STAT_RING[3:0]_LEN
RX_BUF_LEN
CSB_ADDR

Fig. 5C

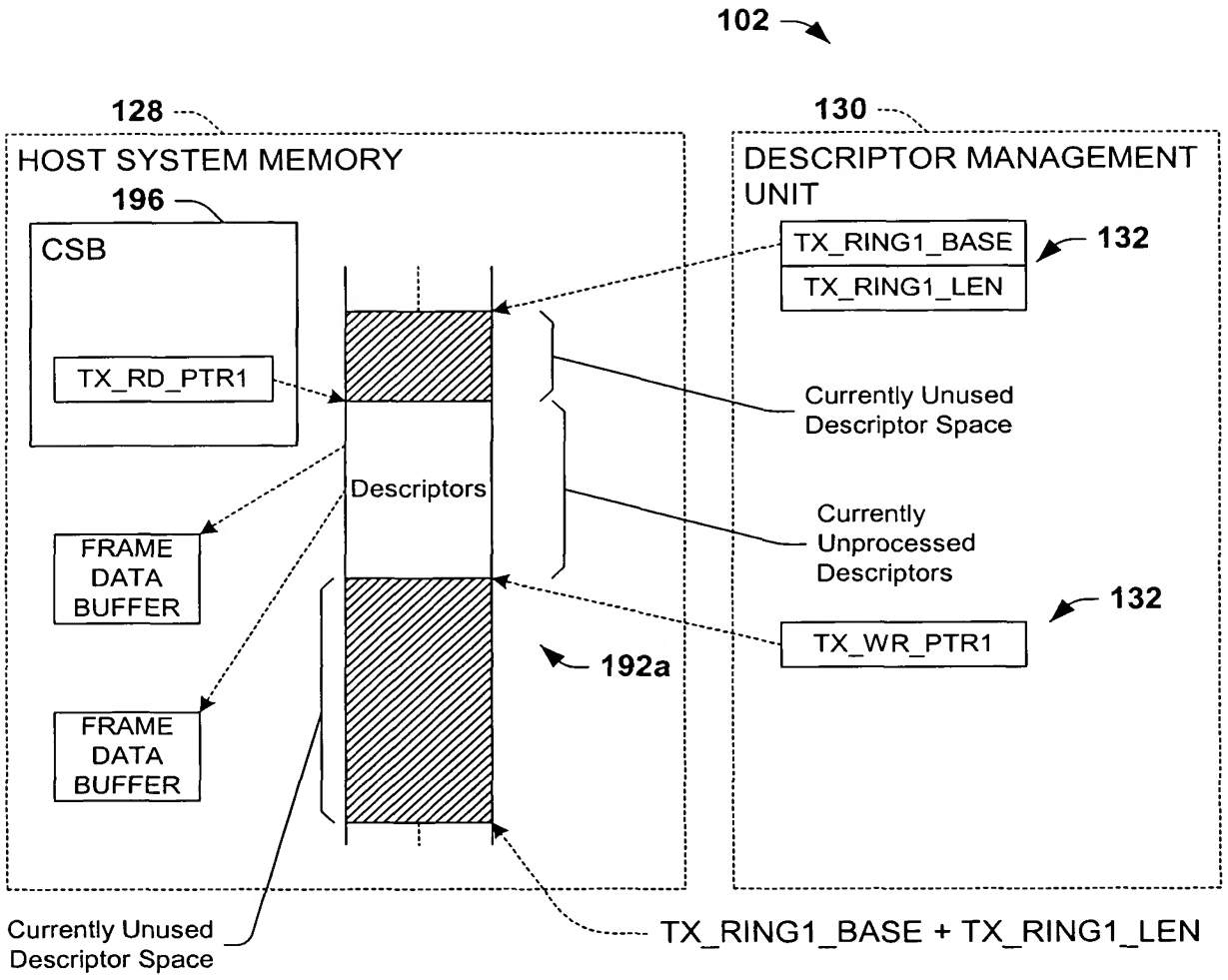
102
128
HOST SYSTEM MEMORY
196
CSB
TX_RD_PTR1
FRAME DATA BUFFER
FRAME DATA BUFFER
Descriptors
Currently Unused Descriptor Space
130
DESCRIPTOR MANAGEMENT UNIT
TX_RING1_BASE
TX_RING1_LEN
132
Currently Unused Descriptor Space
Currently Unprocessed Descriptors
132
TX_WR_PTR1
192a
Currently Unused Descriptor Space
TX_RING1_BASE + TX_RING1_LEN

Fig. 5D

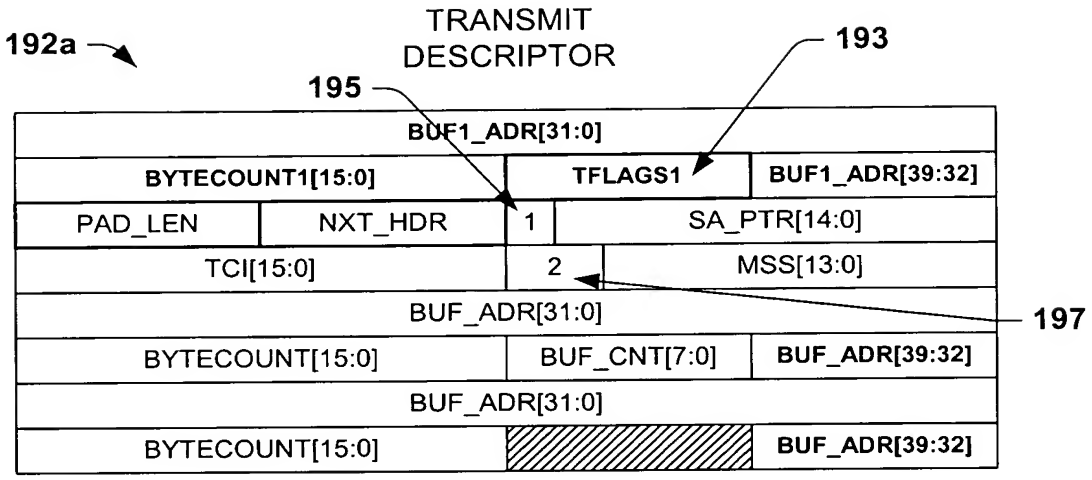

Fig. 5E

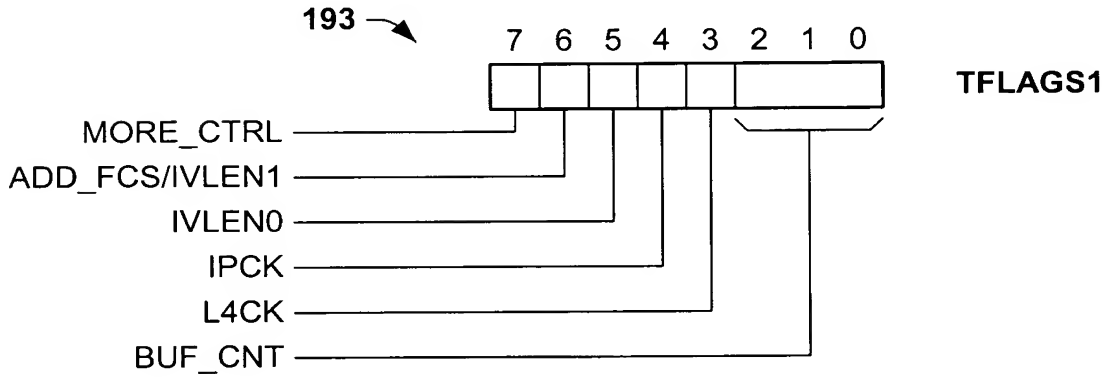

Fig. 5F

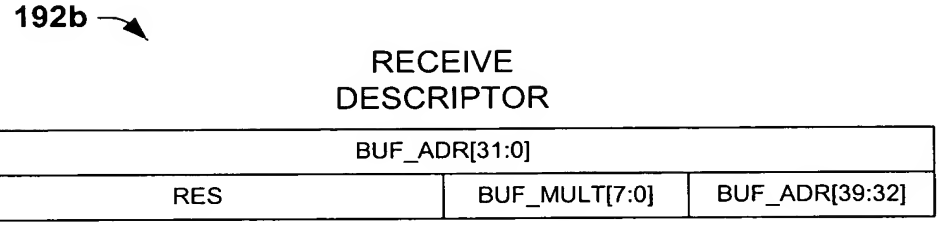

Fig. 5G

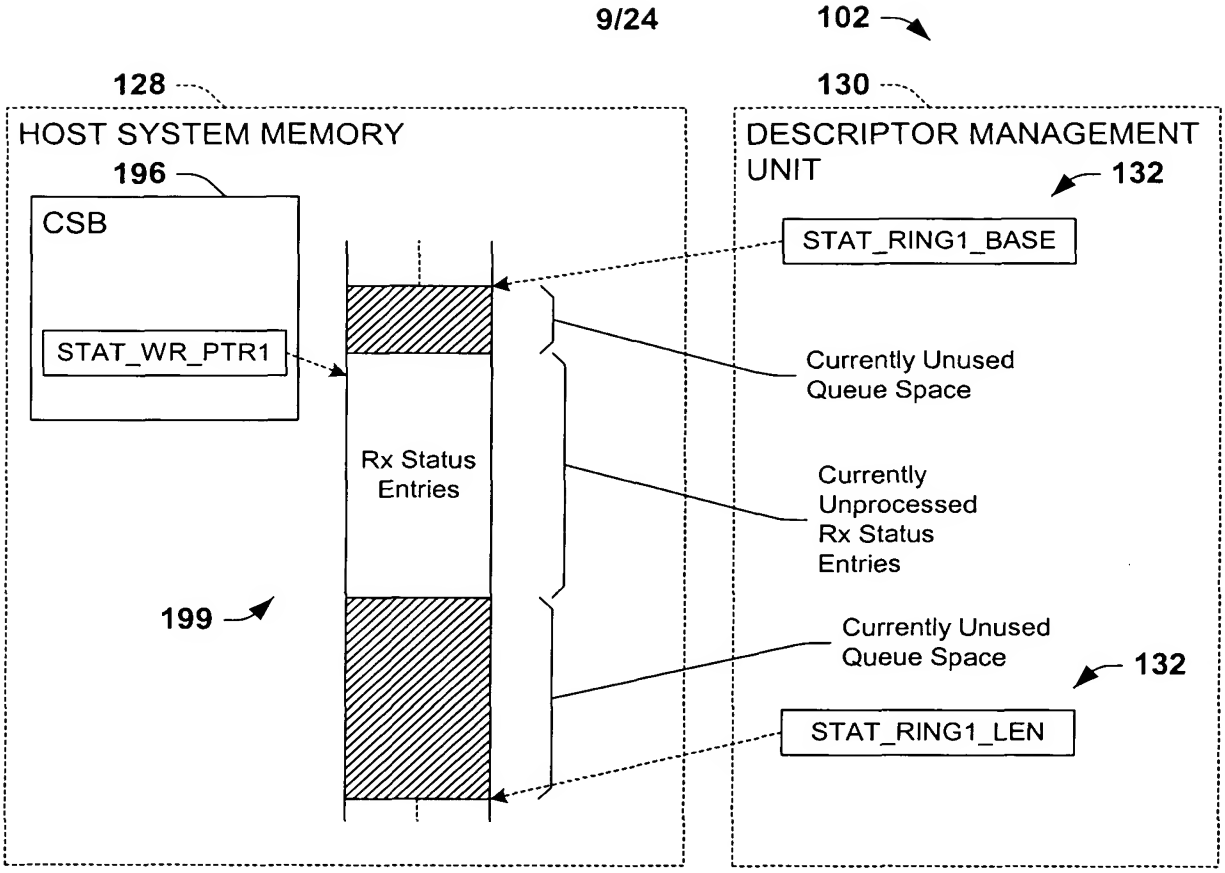
102
128
HOST SYSTEM MEMORY
196
CSB
STAT_WR_PTR1
Rx Status Entries
199
130
DESCRIPTOR MANAGEMENT UNIT
132
STAT_RING1_BASE
Currently Unused Queue Space
Currently Unprocessed Rx Status Entries
Currently Unused Queue Space
132
STAT_RING1_LEN

Fig. 5H

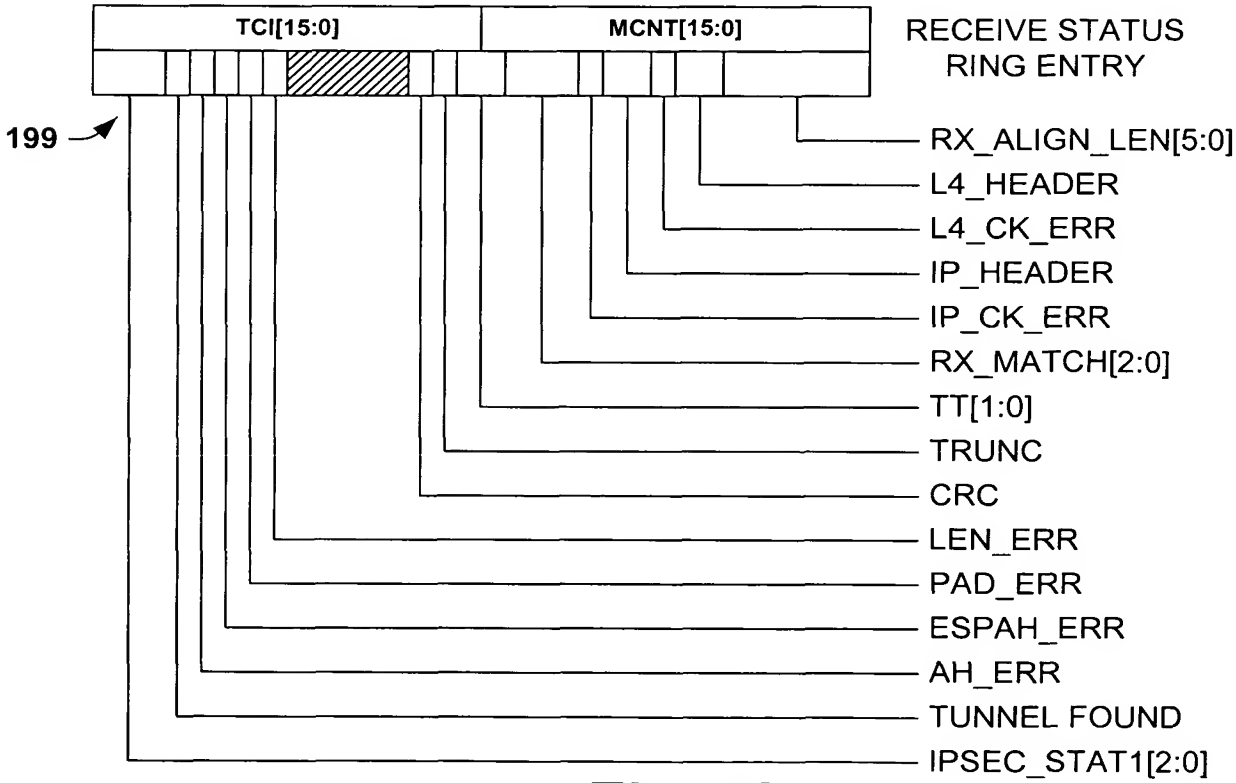
TCI[15:0]
MCNT[15:0]
RECEIVE STATUS RING ENTRY
199
RX_ALIGN_LEN[5:0]
L4_HEADER
L4_CK_ERR
IP_HEADER
IP_CK_ERR
RX_MATCH[2:0]
TT[1:0]
TRUNC
CRC
LEN_ERR
PAD_ERR
ESPAH_ERR
AH_ERR
TUNNEL FOUND
IPSEC_STAT1[2:0]

Fig. 5I

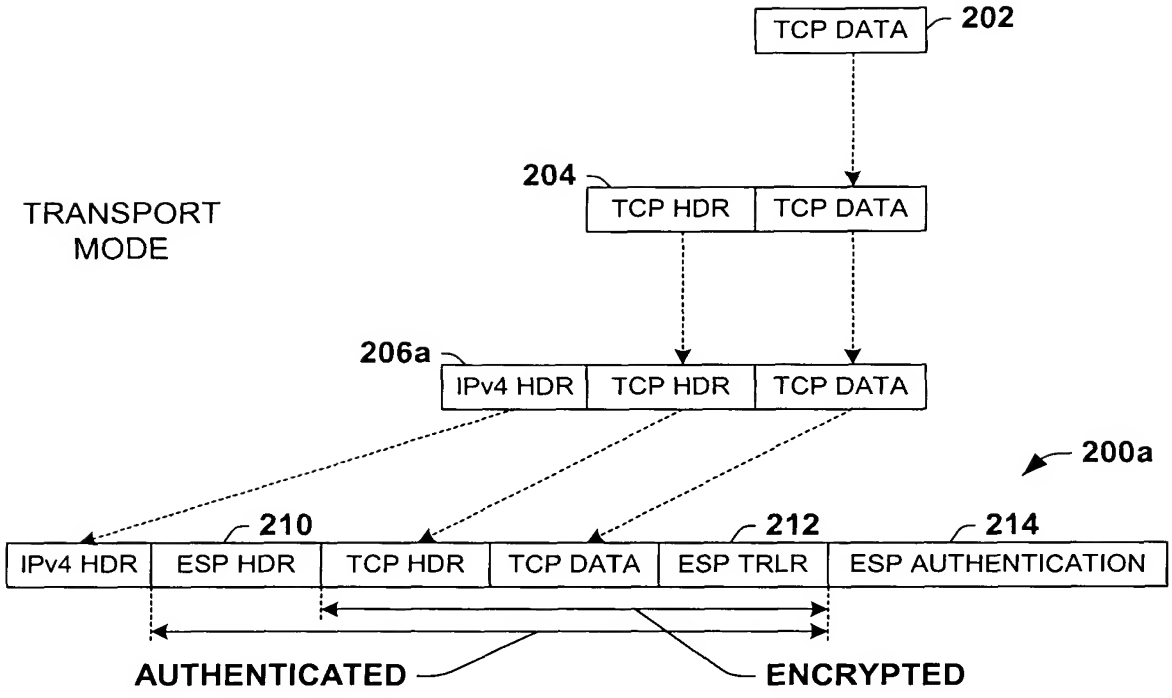
TCP DATA
202
204
TRANSPORT MODE
TCP HDR
TCP DATA
206a
IPv4 HDR
TCP HDR
TCP DATA
200a
210
212
214
IPv4 HDR
ESP HDR
TCP HDR
TCP DATA
ESP TRLR
ESP AUTHENTICATION
AUTHENTICATED
ENCRYPTED

Fig. 6A

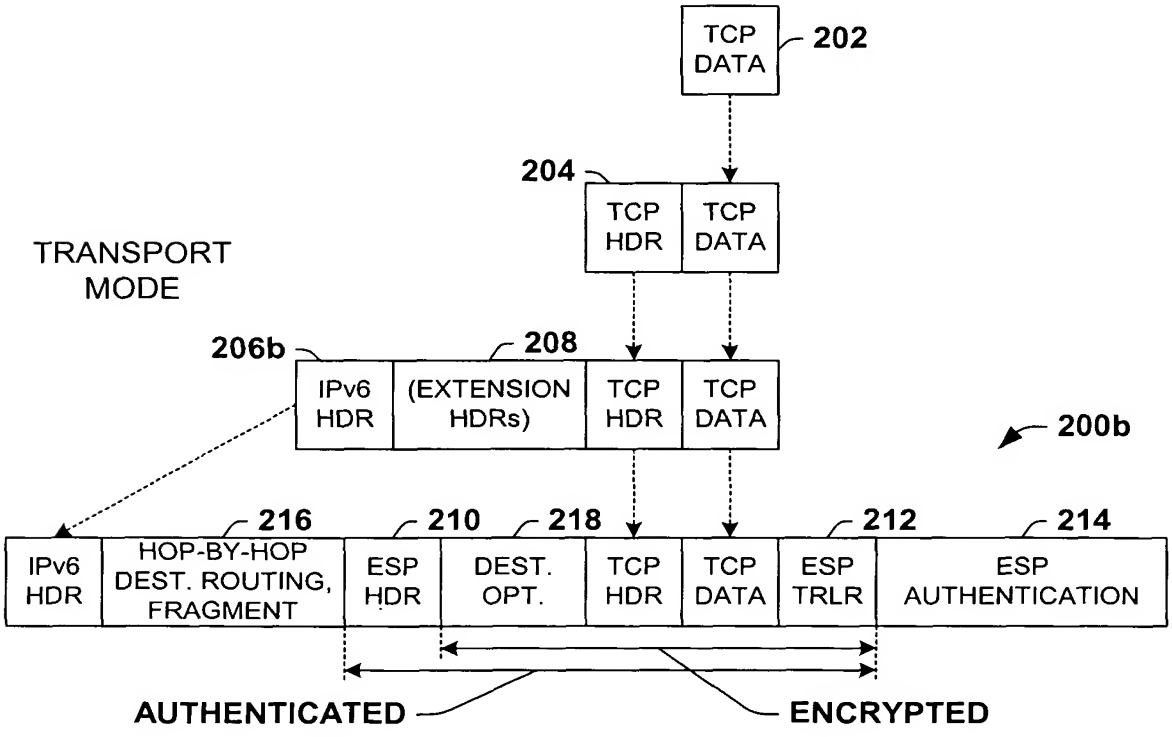
TCP DATA
202
204
TRANSPORT MODE
TCP HDR
TCP DATA
206b
208
IPv6 HDR
(EXTENSION HDRs)
TCP HDR
TCP DATA
200b
216
210
218
212
214
IPv6 HDR
HOP-BY-HOP DEST. ROUTING, FRAGMENT
ESP HDR
DEST. OPT.
TCP HDR
TCP DATA
ESP TRLR
ESP AUTHENTICATION
AUTHENTICATED
ENCRYPTED

Fig. 6B

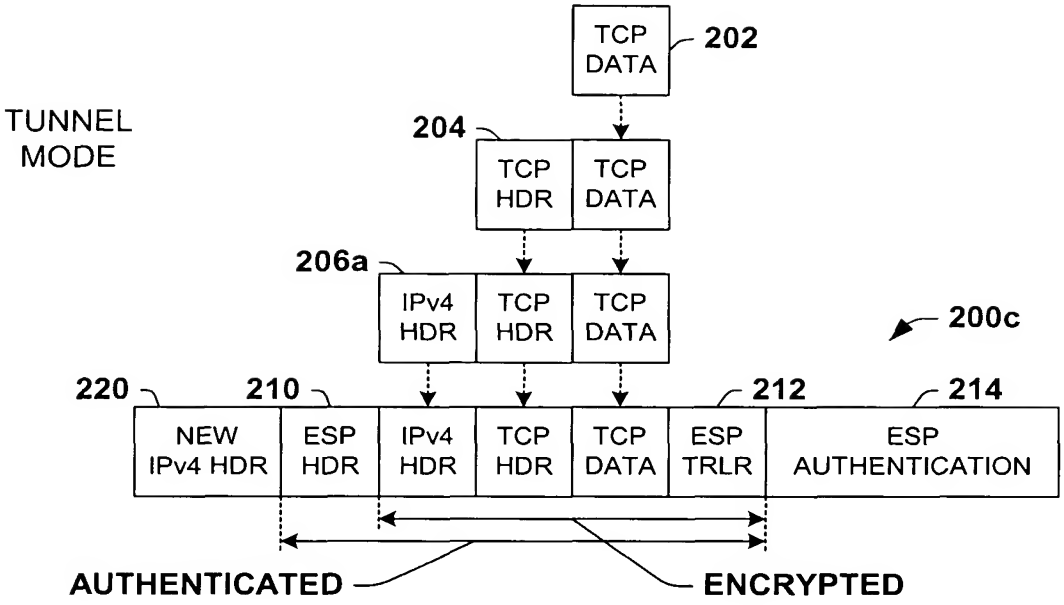
TCP DATA
202
TUNNEL MODE
204
TCP HDR
TCP DATA
206a
IPv4 HDR
TCP HDR
TCP DATA
200c
220
210
212
214
NEW IPv4 HDR
ESP HDR
IPv4 HDR
TCP HDR
TCP DATA
ESP TRLR
ESP AUTHENTICATION
AUTHENTICATED
ENCRYPTED

Fig. 6C

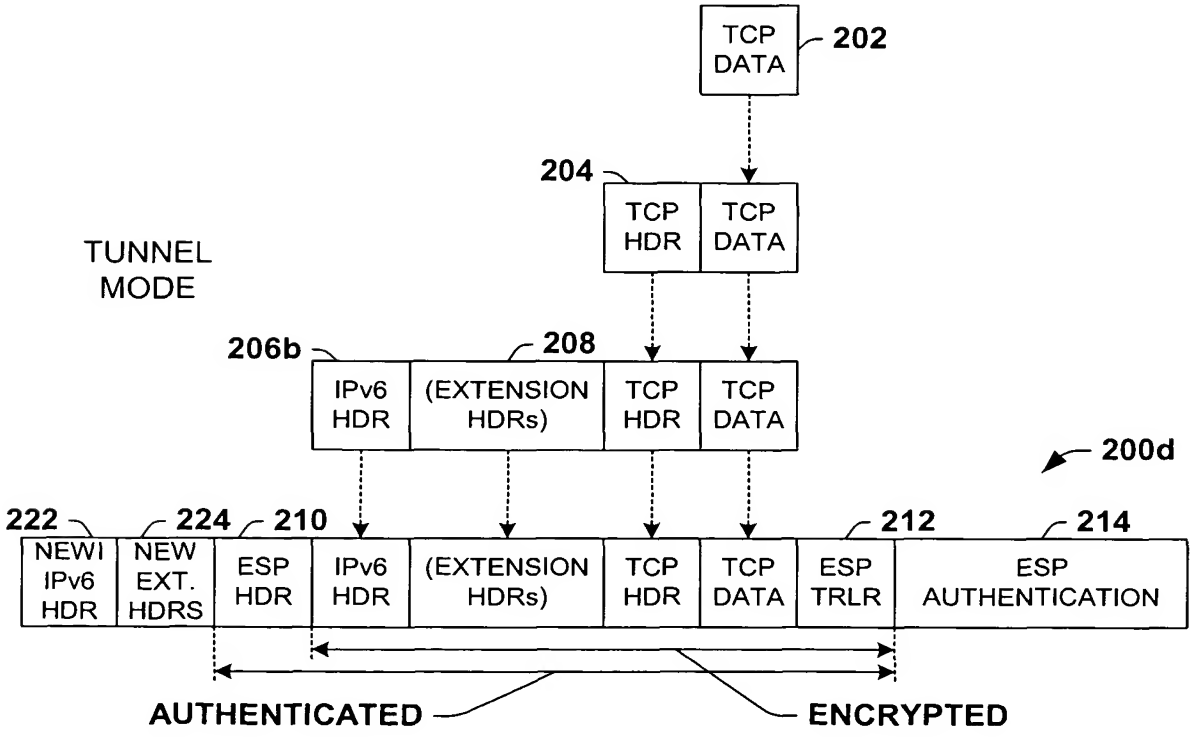
TCP DATA
202
204
TCP HDR
TCP DATA
TUNNEL MODE
206b
208
IPv6 HDR
(EXTENSION HDRs)
TCP HDR
TCP DATA
200d
222
224
210
212
214
NEWI IPv6 HDR
NEW EXT. HDRS
ESP HDR
IPv6 HDR
(EXTENSION HDRs)
TCP HDR
TCP DATA
ESP TRLR
ESP AUTHENTICATION
AUTHENTICATED
ENCRYPTED

Fig. 6D

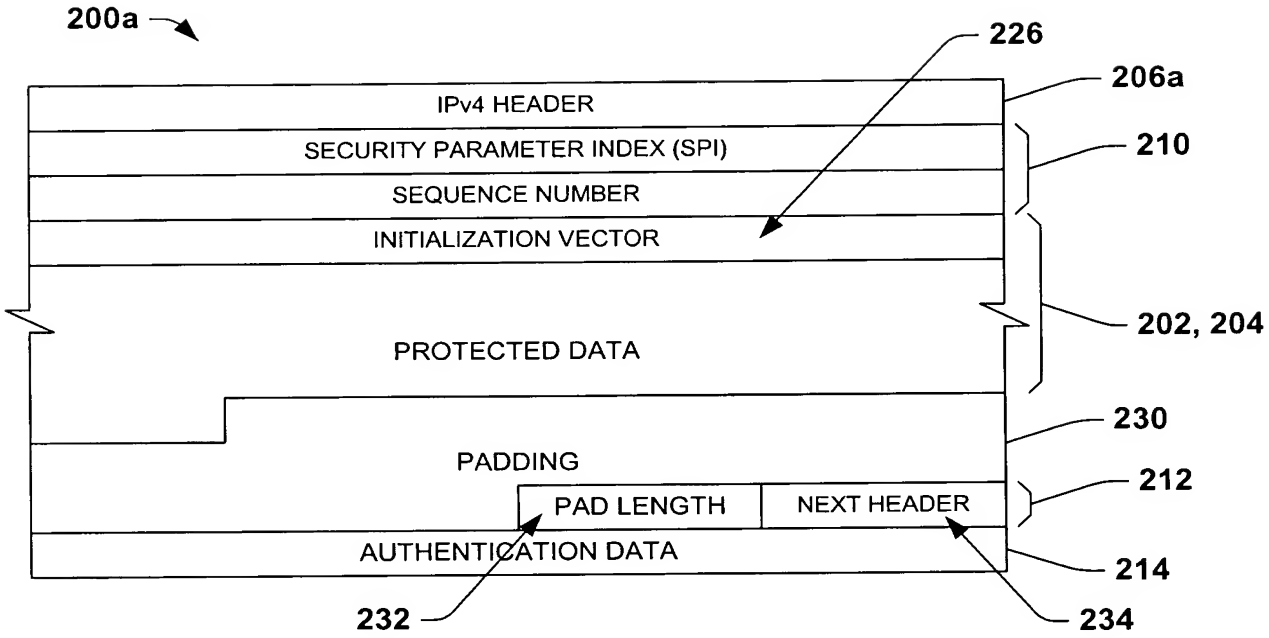
200a
226
206a
IPv4 HEADER
SECURITY PARAMETER INDEX (SPI)
SEQUENCE NUMBER
INITIALIZATION VECTOR
210
PROTECTED DATA
202, 204
230
PADDING
PAD LENGTH
NEXT HEADER
212
AUTHENTICATION DATA
214
232
234

Fig. 6E

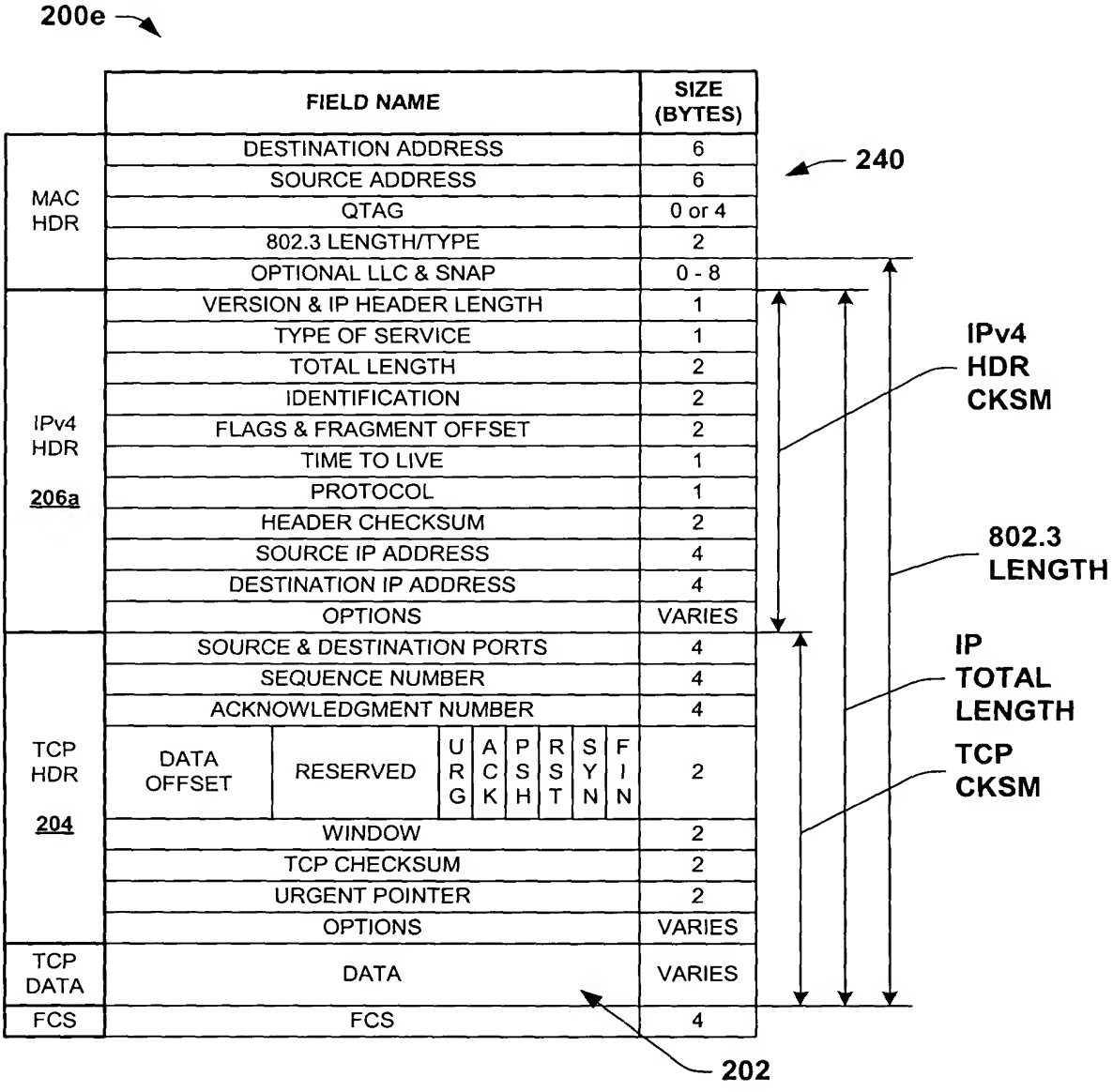
200e
FIELD NAME
SIZE (BYTES)
MAC HDR
DESTINATION ADDRESS 6
SOURCE ADDRESS 6
QTAG 0 or 4
802.3 LENGTH/TYPE 2
OPTIONAL LLC & SNAP 0 - 8
240
IPv4 HDR
206a
VERSION & IP HEADER LENGTH 1
TYPE OF SERVICE 1
TOTAL LENGTH 2
IDENTIFICATION 2
FLAGS & FRAGMENT OFFSET 2
TIME TO LIVE 1
PROTOCOL 1
HEADER CHECKSUM 2
SOURCE IP ADDRESS 4
DESTINATION IP ADDRESS 4
OPTIONS VARIES
IPv4 HDR CKSM
802.3 LENGTH
TCP HDR
204
SOURCE & DESTINATION PORTS 4
SEQUENCE NUMBER 4
ACKNOWLEDGMENT NUMBER 4
DATA OFFSET
RESERVED
URG ACK PSH RST SYN FIN
2
WINDOW 2
TCP CHECKSUM 2
URGENT POINTER 2
OPTIONS VARIES
IP TOTAL LENGTH
TCP CKSM
TCP DATA
DATA VARIES
FCS
FCS 4
202

Fig. 7A

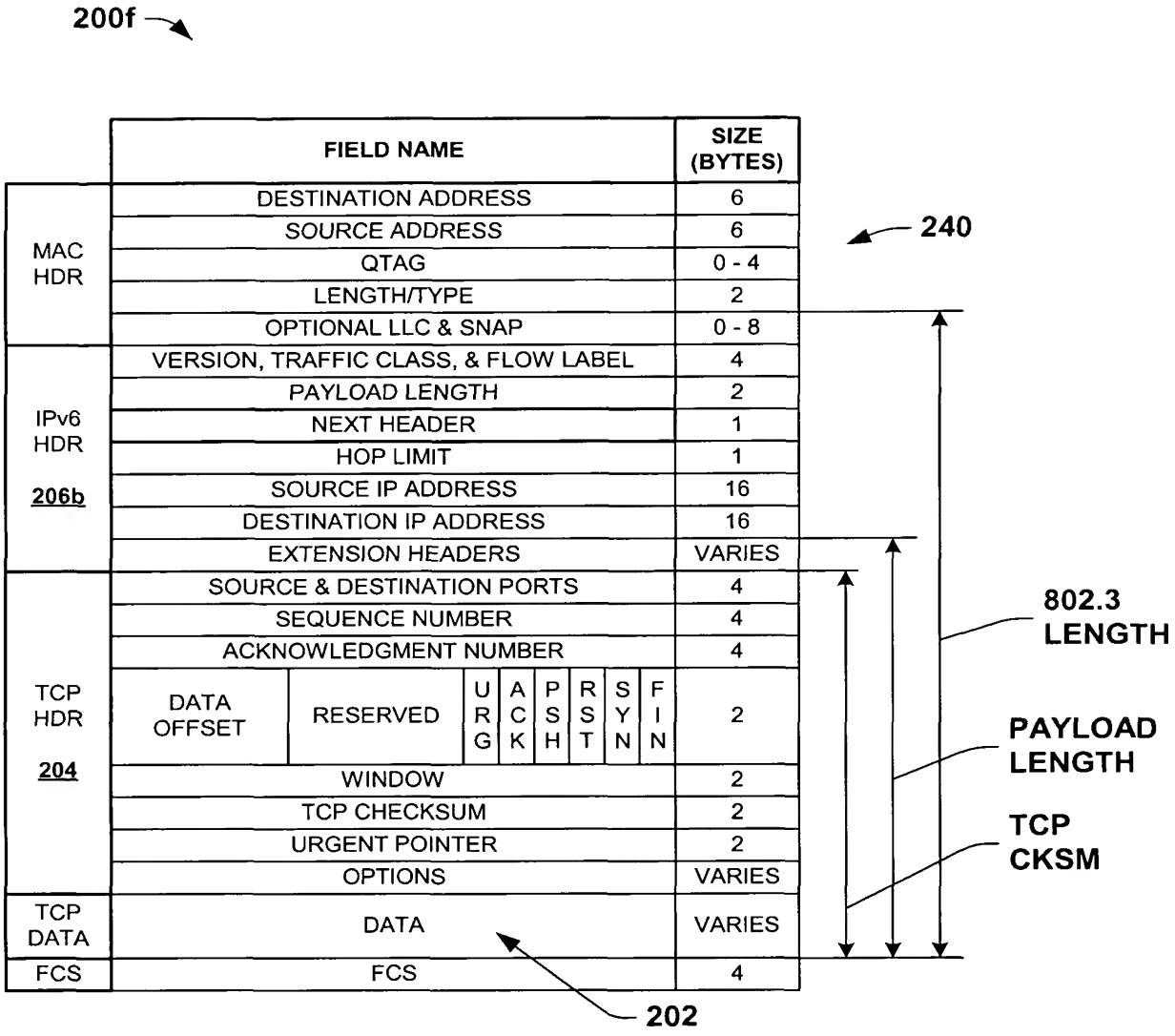
200f
FIELD NAME
SIZE (BYTES)
MAC HDR
DESTINATION ADDRESS 6
SOURCE ADDRESS 6
QTAG 0 - 4
LENGTH/TYPE 2
OPTIONAL LLC & SNAP 0 - 8
IPv6 HDR
206b
VERSION, TRAFFIC CLASS, & FLOW LABEL 4
PAYLOAD LENGTH 2
NEXT HEADER 1
HOP LIMIT 1
SOURCE IP ADDRESS 16
DESTINATION IP ADDRESS 16
EXTENSION HEADERS VARIES
TCP HDR
204
SOURCE & DESTINATION PORTS 4
SEQUENCE NUMBER 4
ACKNOWLEDGMENT NUMBER 4
DATA OFFSET
RESERVED
URG ACK PSH RST SYN FIN
2
WINDOW 2
TCP CHECKSUM 2
URGENT POINTER 2
OPTIONS VARIES
TCP DATA
DATA VARIES
FCS
FCS 4
240
802.3 LENGTH
PAYLOAD LENGTH
TCP CKSM
202

Fig. 7B

250

FIELD NAME	Created by Host	Modified by ESP	Encrypted	Covered by ESP Authentication	Added by Controller
Preamble					x
Start of Frame Delimiter					x
MAC Header	x				
IP Header	x				
ESP Header	x			x	
Payload Data	x	x	x	x	
Padding	x	x	x	x	
Pad Length	x	x	x	x	
Next Header	x	x	x	x	
Authentication Data	x	x			
Frame Check Sequence					x

Fig. 8A

252

FIELD NAME	Created by Host	Modified by AH Module	Covered by AH Authentication	Added by Controller
Preamble				x
Start of Frame Delimiter				x
MAC Header	x			
IP Header	x		x	
AH Header	x	x	x	
Other Headers	x		x	
Payload Data	x		x	
Frame Check Sequence				X

Fig. 8B

254

PHCKSM FOR IPv4	
32-BIT IP SOURCE ADDRESS	
32-BIT IP DESTINATION ADDRESS	
ZERO	PROTOCOL
TCP TOTAL LENGTH	

Fig. 8C

256

PHCKSM FOR IPv6	
128-BIT IP SOURCE ADDRESS	
128-BIT IP DESTINATION ADDRESS	
16-BIT TCP TOTAL LENGTH	
ZERO	PROTOCOL

Fig. 8D

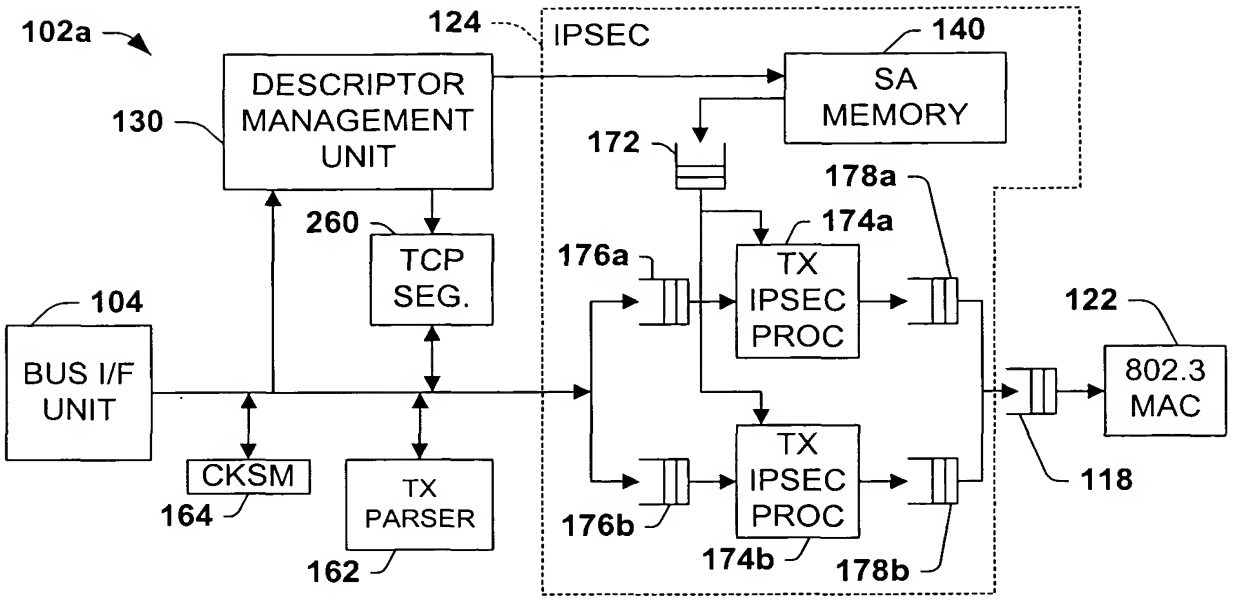
102a
124
IPSEC
140
SA MEMORY
DESCRIPTOR MANAGEMENT UNIT
130
172
178a
174a
260
TCP SEG.
176a
TX IPSEC PROC
104
122
BUS I/F UNIT
802.3 MAC
CKSM
164
TX PARSER
162
176b
TX IPSEC PROC
174b
178b
118

Fig. 9

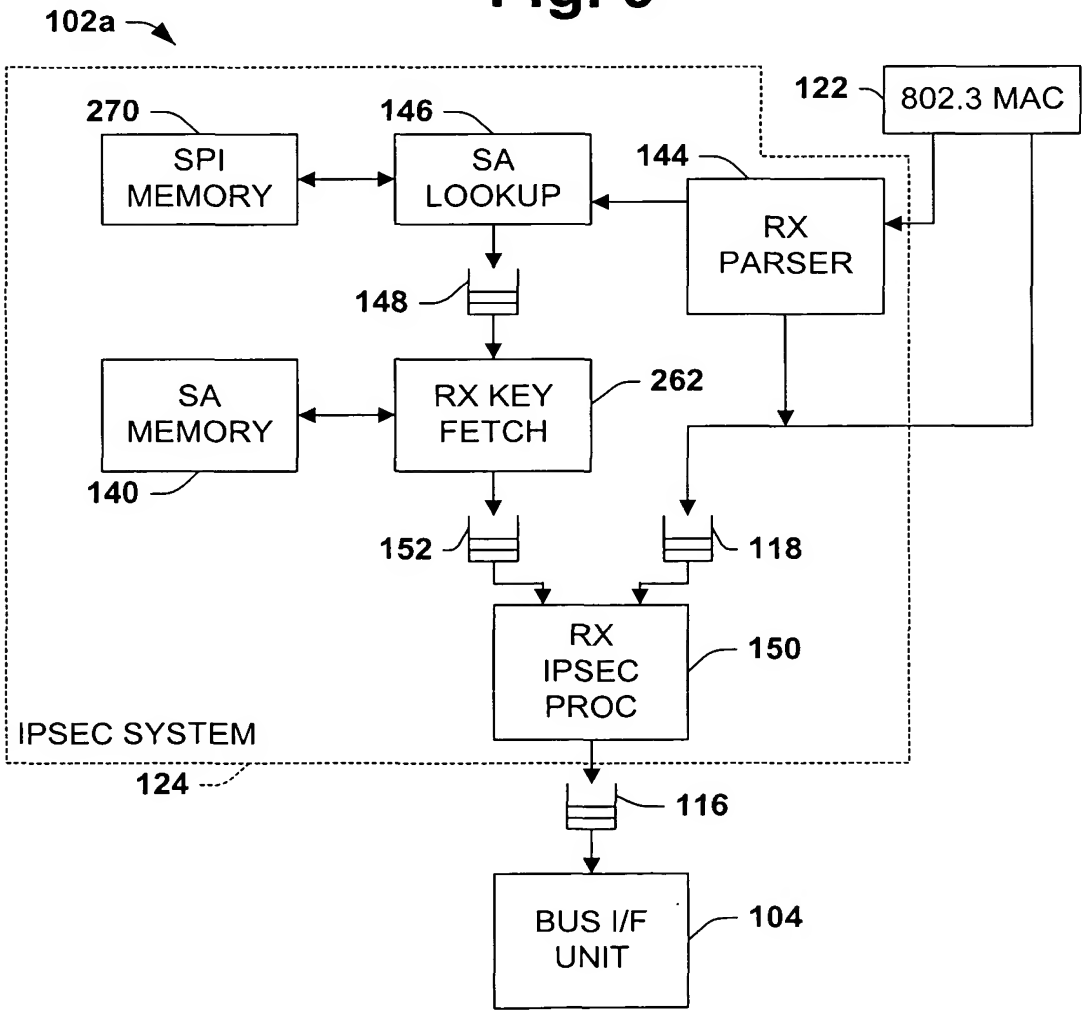
102a
122
802.3 MAC
270
SPI MEMORY
146
SA LOOKUP
144
RX PARSER
148
SA MEMORY
140
RX KEY FETCH
262
152
118
RX IPSEC PROC
150
IPSEC SYSTEM
124
116
BUS I/F UNIT
104

Fig. 10

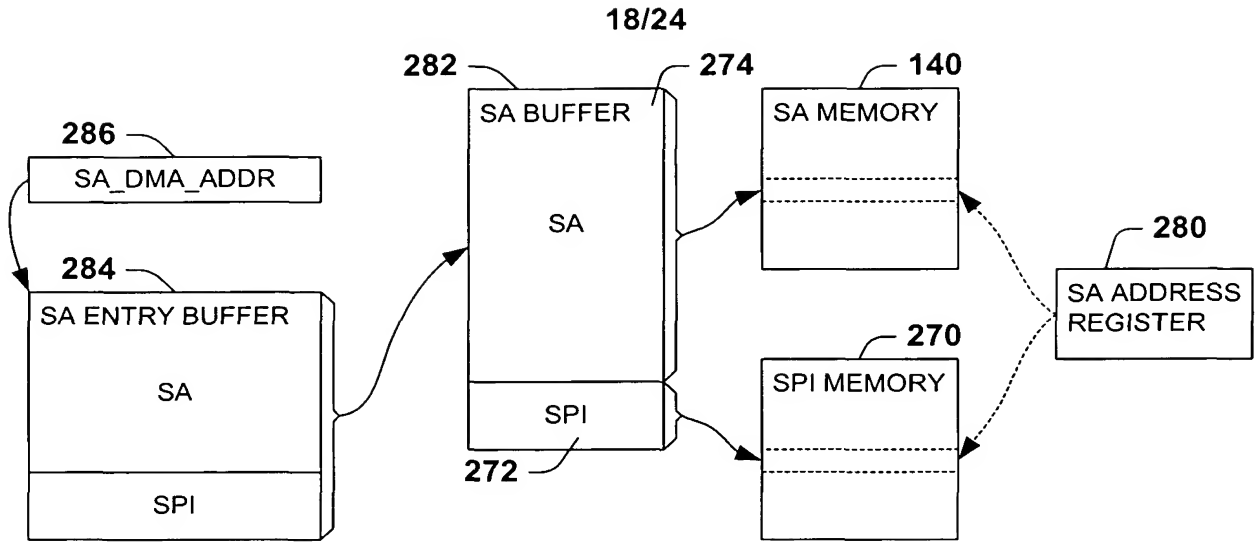

Fig. 11A

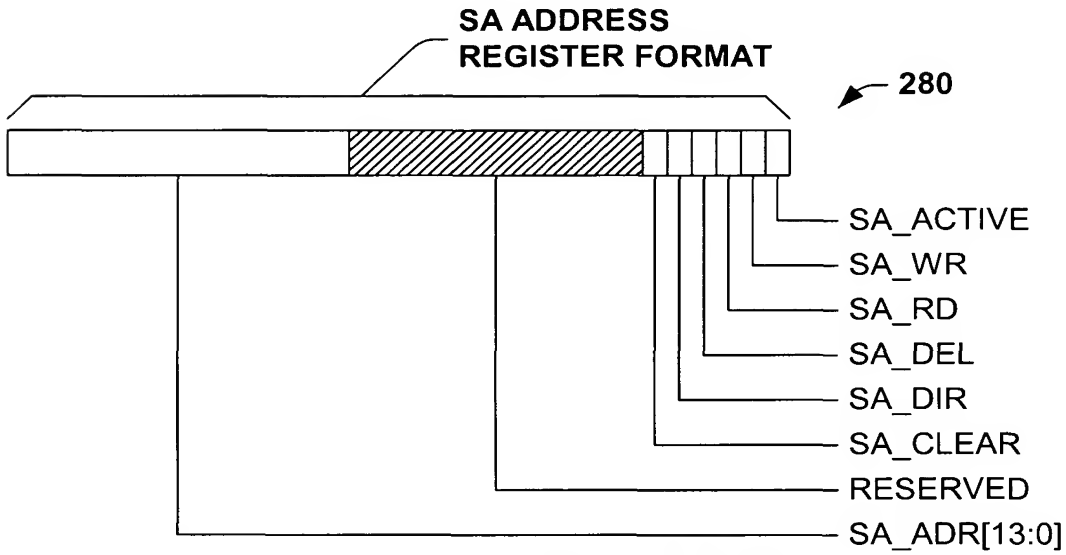

Fig. 11B

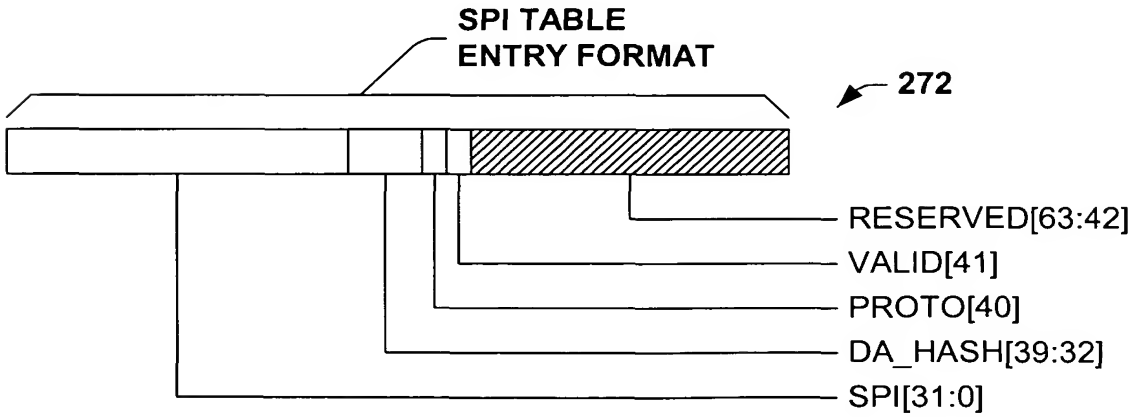

Fig. 11C

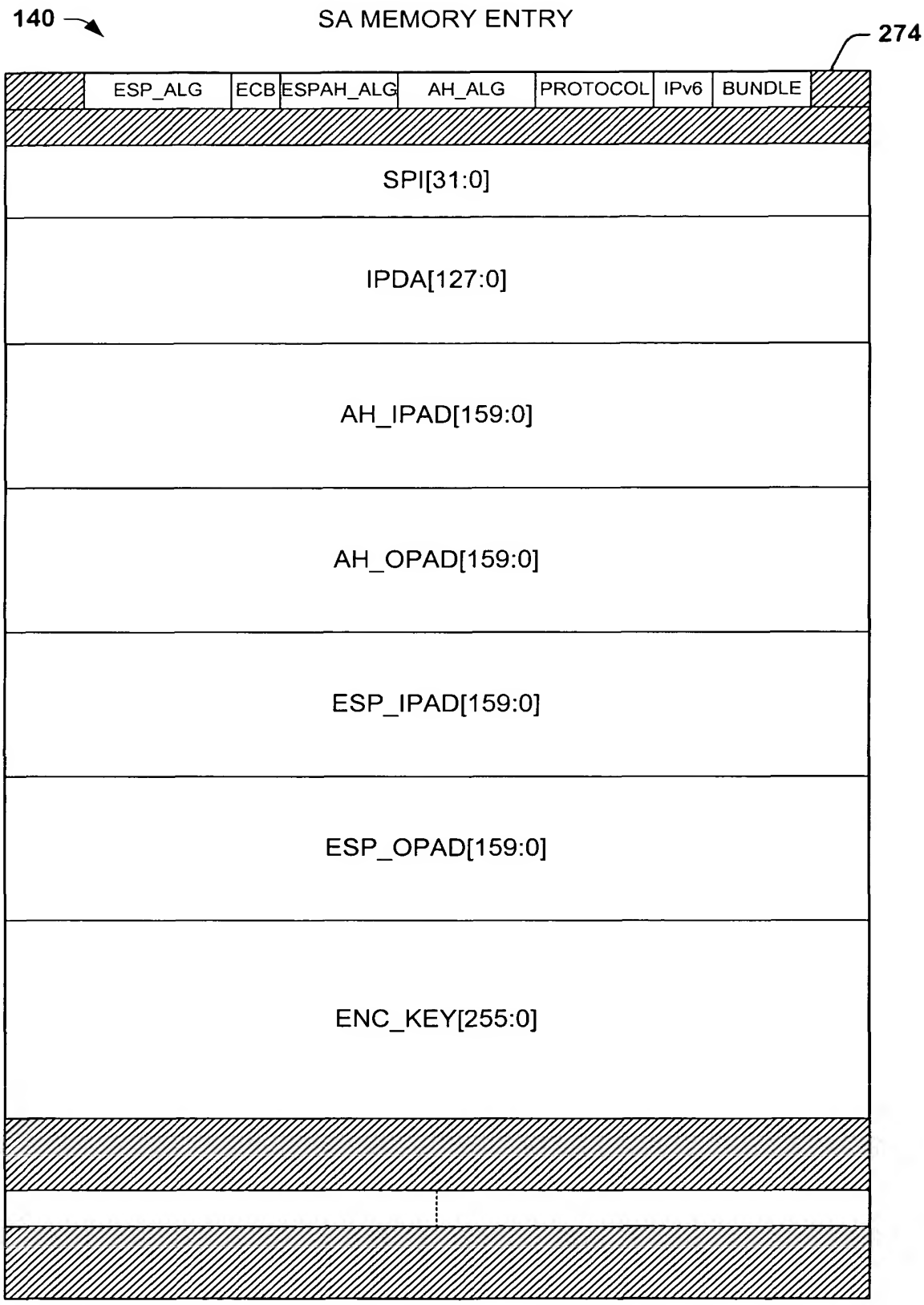
140
SA MEMORY ENTRY
274
ESP_ALG
ECB
ESPAH_ALG
AH_ALG
PROTOCOL
IPv6
BUNDLE
SPI[31:0]
IPDA[127:0]
AH_IPAD[159:0]
AH_OPAD[159:0]
ESP_IPAD[159:0]
ESP_OPAD[159:0]
ENC_KEY[255:0]

Fig. 11D

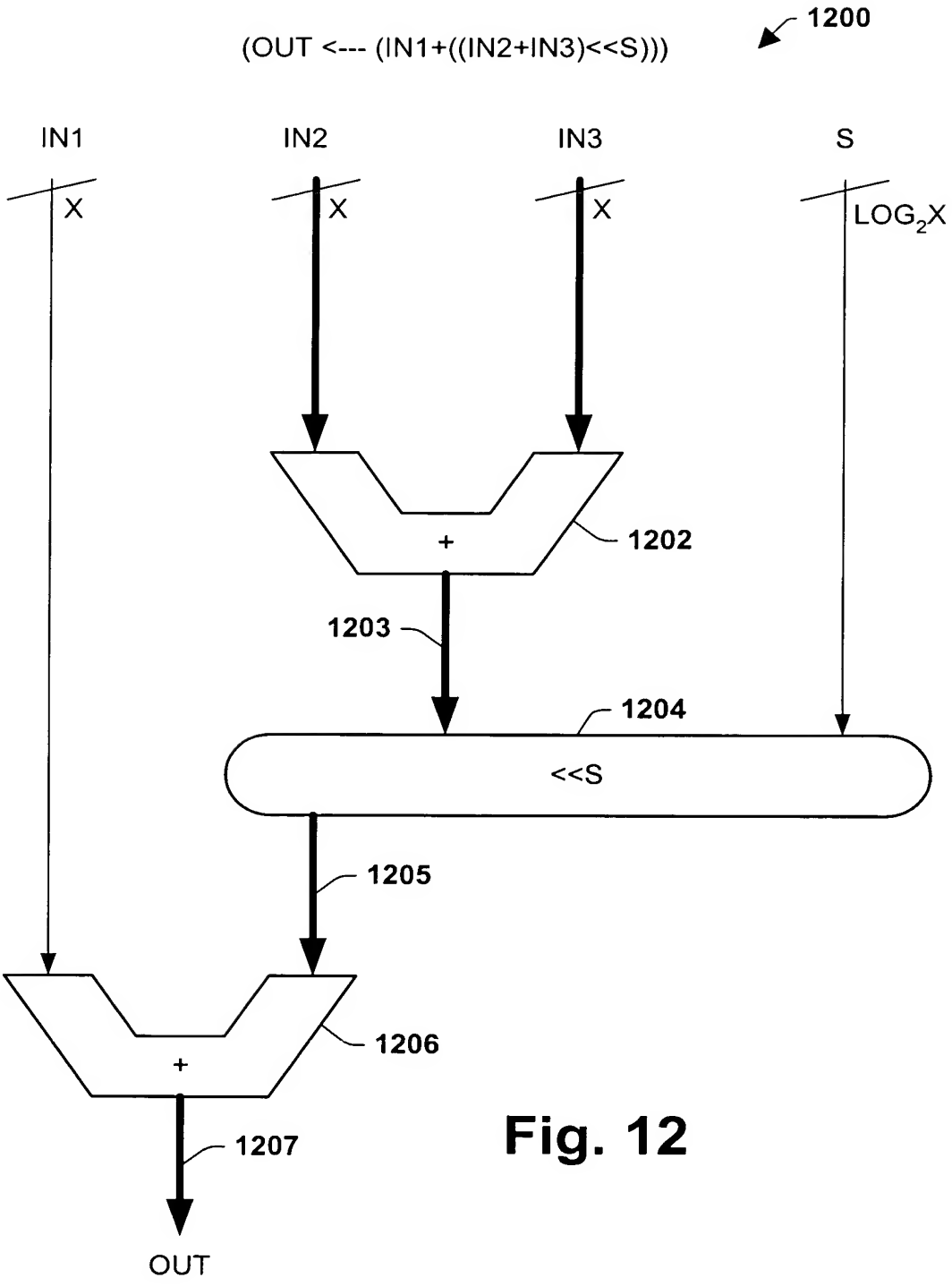
1200
(OUT <--- (IN1+((IN2+IN3)<<S)))
IN1
IN2
IN3
S
X
X
X
LOG2X
+
1202
1203
1204
<<S
1205
+
1206
1207
OUT

Fig. 12

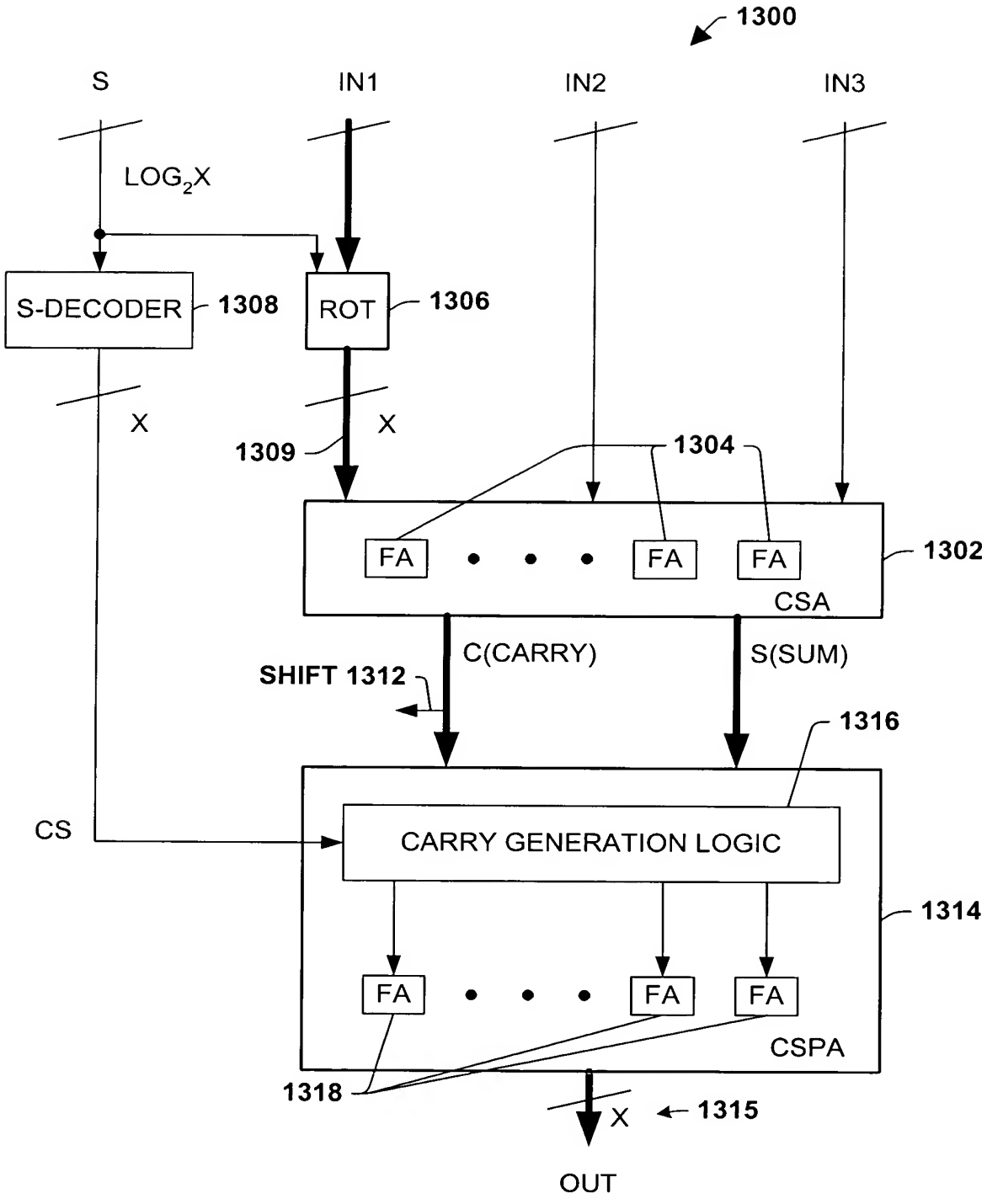
1300
S
IN1
IN2
IN3
LOG2X
S-DECODER
1308
ROT
1306
X
X
1309
1304
FA
FA
FA
1302
CSA
C(CARRY)
S(SUM)
SHIFT 1312
1316
CS
CARRY GENERATION LOGIC
1314
FA
FA
FA
CSPA
1318
X
1315
OUT

Fig. 13

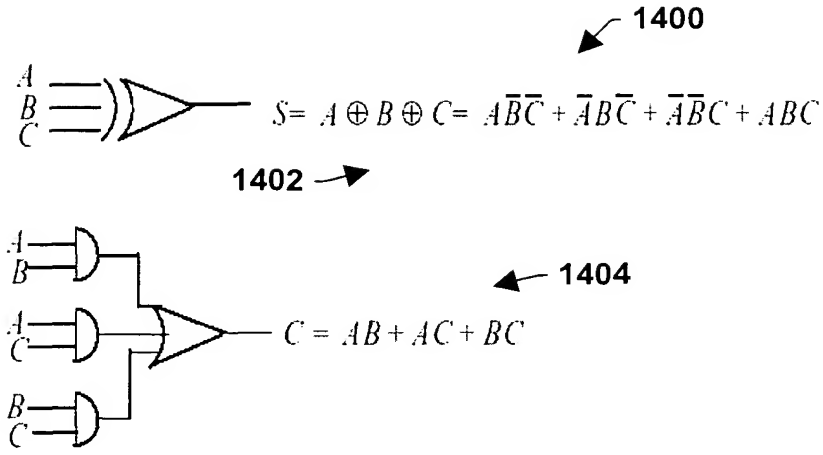

Fig. 14

1500

INPUTS			OUTPUTS	
A	B	C_{IN}	C_{OUT}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig. 15

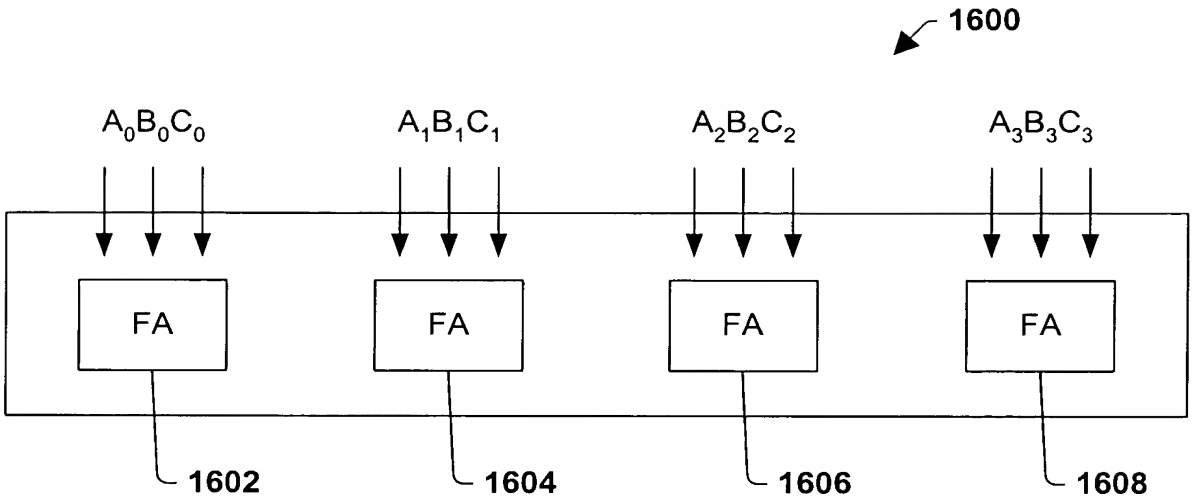
1600
$A_0B_0C_0$
$A_1B_1C_1$
$A_2B_2C_2$
$A_3B_3C_3$
FA
FA
FA
FA
1602
1604
1606
1608

Fig. 16

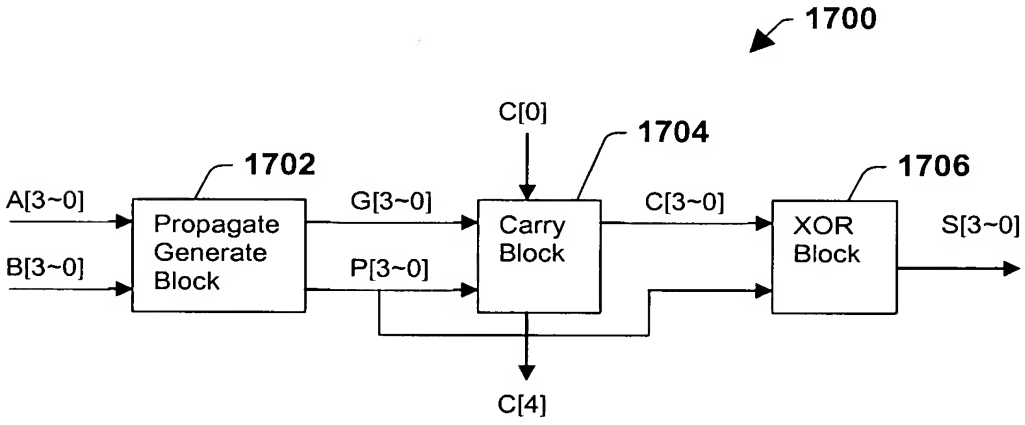
1700
C[0]
1704
1702
1706
A[3~0]
B[3~0]
Propagate Generate Block
G[3~0]
P[3~0]
Carry Block
C[3~0]
XOR Block
S[3~0]
C[4]

Fig. 17

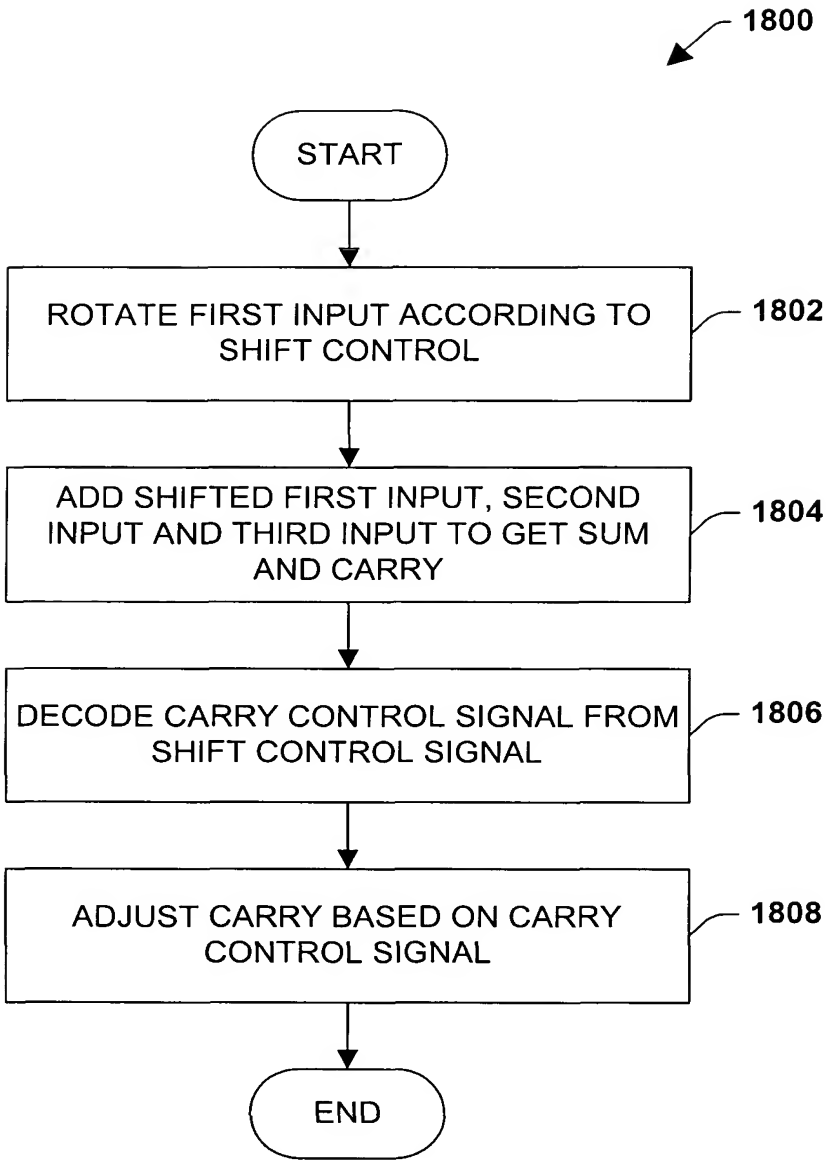
1800
START
ROTATE FIRST INPUT ACCORDING TO SHIFT CONTROL
1802
ADD SHIFTED FIRST INPUT, SECOND INPUT AND THIRD INPUT TO GET SUM AND CARRY
1804
DECODE CARRY CONTROL SIGNAL FROM SHIFT CONTROL SIGNAL
1806
ADJUST CARRY BASED ON CARRY CONTROL SIGNAL
1808
END

Fig. 18